

Features

- GaN-on Silicon E-mode HEMT technology
- Very low gate charge
- Ultra low On-resistance
- Very small footprint

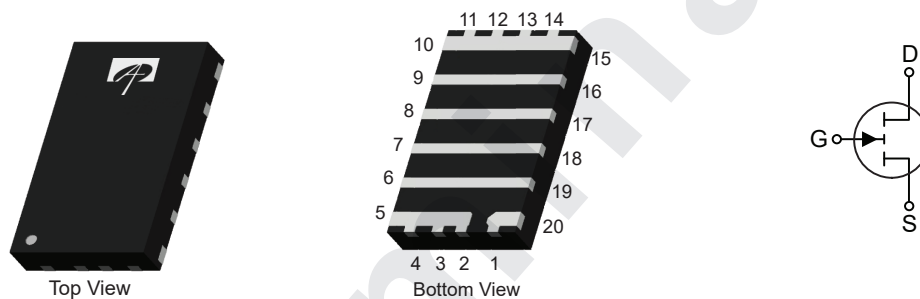
Applications

- High frequency DC/DC converter
- BMS protection
- RF envelope tracking
- PC charger and mobile power bank
- Motor driver

Product Summary at $T_J = 25^\circ\text{C}$

$V_{DS, \text{max}}$	100V
$R_{DS(\text{on}), \text{max}} @ V_{GS} = 5V$	2.8m Ω
$Q_g, \text{typ} @ V_{DS} = 50V$	14nC
$I_{DS, \text{Pulse}}$	320A
$Q_{oss} @ V_{DS} = 50V$	85nC

Pin Configuration



Pin Information

Pin	Pin Description	Pin Function
1, 20	Gate	Driver Gate
2-5, 7, 9, 16, 18	Source	Source
6, 8, 10-15, 17, 19	Drain	Power Drain

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AOFQ028V10GA1	FCQFN3x5	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

($T_J = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	AOFQ028V10GA1	Units
V_{DS}	Drain-Source Voltage (Continuous)	100	V
$V_{DS(\text{tr})}$	Drain-Source Voltage (up to 300,000 5ms pulse at 150°C)	120	
I_D	Continuous Drain Current	80	A
	Pulsed (25°C , $T_{\text{Pulse}} = 100\mu\text{s}$)	320	
V_{GS}	Gate-Source Voltage	-4 to 6	V
$T_{j, \text{stg}}$	Operating and Storage Temperature	-40 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Note	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient ⁽¹⁾	61.06			°C/W
$R_{\theta JB}$	Thermal Resistance Junction-to-Board	1.89			°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	14.15			°C/W
T_{sold}	Maximum Reflow Soldering Temperature	260		MSL3	°C

Electrical Characteristics

($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

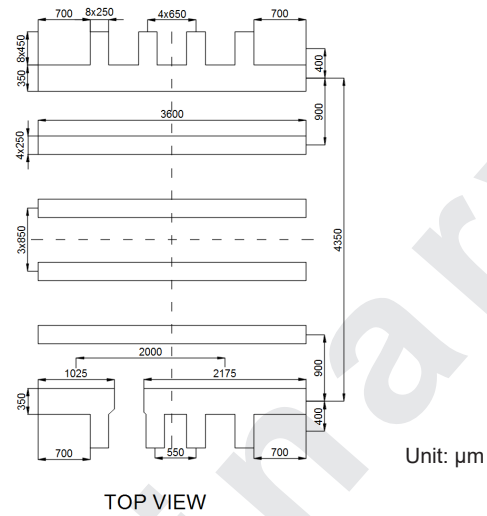
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 600\mu\text{A}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		12	24	μA
I_{GSS}	Gate-Source Forward Leakage	$V_{GS} = 5\text{ V}$		2.5	9	μA
	Gate-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.3	0.5	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 13\text{ mA}$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On-State-Resistance	$V_{GS} = 5\text{ V}, I_D = 30\text{ A}$		2.2	2.8	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.5		V
DYNAMIC						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		1500		pF
C_{OSS}	Output Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		700		
C_{RSS}	Reverse Transfer Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		12.5		
$C_{OSS(ER)}$	Energy Related C_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 50\text{ V}$		1150		
$C_{OSS(TR)}$	Time Related C_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 50\text{ V}$		1600		
R_G	Gate Resistance	$f = 5\text{ MHz}, \text{open drain}$		1.8		Ω
Q_G	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 50\text{ V}, I_D = 30\text{ A}$		14		nC
Q_{GS}	Gate-Source Charge	$V_{DS} = 50\text{ V}, I_D = 30\text{ A}$		2.8		
Q_{GD}	Gate-Drain Charge	$V_{DS} = 50\text{ V}, I_D = 30\text{ A}$		3		
$Q_{G(TH)}$	Gate Charge at Threshold	$V_{DS} = 50\text{ V}, I_D = 30\text{ A}$		1.5		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		85		

Note:

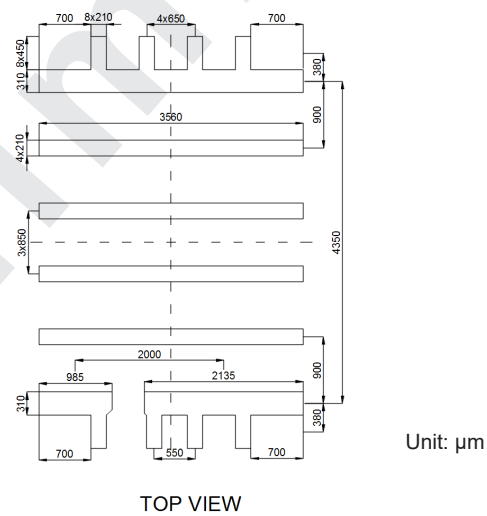
1. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

Land Pattern, FCQFN3x5

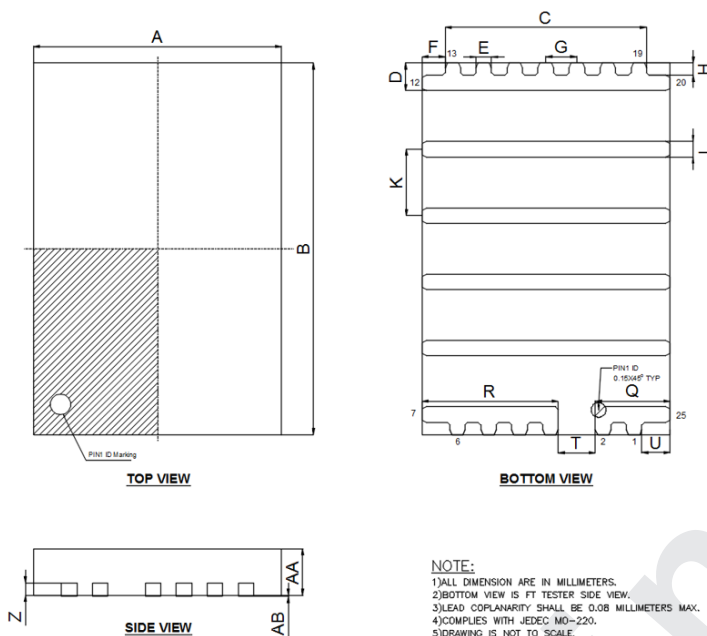
Recommended land pattern



Recommended Stencil drawing

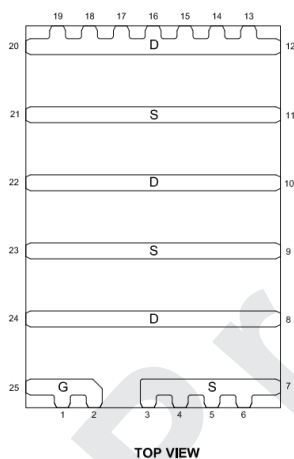


Package Dimensions, FCQFN3x5



SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
C	3.15	3.25	3.35	
D	0.35	0.45	0.55	3X
E	0.20	0.25	0.30	13X
F		0.375 REF		2X
G		0.5 BASIC		10X
H		0.2 REF		3X
K		1.07 BASIC		6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
T	0.55	0.60	0.65	
U		0.45 REF		2X
Z		0.203 REF		7X
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	

PIN Configuration



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