ALPHA & OMEGA SEMICONDUCTOR

AONS190V70GA1

700V GaN Enhancement-mode Power Transistor

Features

- 700V GaN enhancement-mode transistor
- Normally-off design
- No Qrr (reverse recovery charge)
- Low Qg (gate charge), low Qoss (output charge)
- Integrated ESD protection

Applications

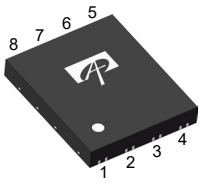
- PFC and PWM stages (LLC, FSFB, TTF) of Server, Telecom, Industrial, UPS, and Solar Inverters

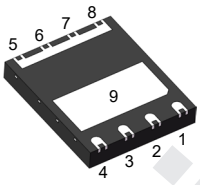
Product Summary at T_J = 25°C

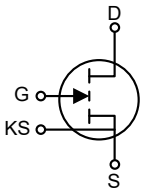
$V_{DS,\ max}$	700V
$R_{DS(on),\ max}$ @ V_{GS} = 6V	190mΩ
$Q_{g,\ typ}$ @ V_{DS} = 400V	2.8nC
$I_{D,\ pulse}$	20.5A
Q_{oss} @ V_{DS} = 400V	24.5nC
Q_{rr} @ V_{DS} = 400V	0nC

RoHS Compliant

Pin Configuration







Pin Information

Gate	Drain	Kelvin Source	Source
4	5, 6, 7, 8	3	1, 2, 9

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AONS190V70GA1	DFN5x6	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AONS190V70GA1	Units
$V_{DS,\ max}$	Drain Source Voltage	V_{GS}=0V, T_J=-55°C to 150°C	700	V
$V_{DS,\ trans}$	Drain Source Voltage Transient (1)	V_{GS}=0V	800	
$V_{DS,\ pulse}$	Drain Source Voltage Pulsed (2)	T_C=25°C, total time < 10 hours	750	
		T_C=125°C, total time < 1 hour		
I_D	Continuous Drain Current	T_C=25°C	11.5	A
$I_{D,\ pulse}$	Pulsed Drain Current (3)	T_C=25°C, V_{GS}=6V, t_{pulse}=10µs	20.5	
		T_C=125°C, V_{GS}=6V, t_{pulse}=10µs	11.5	

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

V_{GS}	Gate Source Voltage, Continuous	T_J = -55°C to 150°C	-6 to 7	V
$V_{GS, pulse}$	Gate Source Voltage, Pulsed	T_J = -55°C to 150°C, t_{pulse} = 50ns, f = 100kHz, open drain	-20 to 10	V
P_{tot}	Power Dissipation (4)	T_C = 25°C	82	W
$T_{j, stg}$	Junction and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Note	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (5)	70			°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	1.52	1.86		°C/W
T_{sold}	Maximum Reflow Soldering Temperature	260		MSL3	°C

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=12.2mA	T_J=25°C	1.2	1.7	2.5	V
			T_J=150°C		1.7		
I_{DSS}	Drain-Source Leakage Current	V_{DS}=700V, V_{GS}=0V	T_J=25°C		0.45	20	µA
			T_J=150°C		6		
I_{GSS}	Gate-Source Leakage Current	V_{GS}=6V, V_{DS}=0V, T_j=25°C			60		µA
$R_{DS(on)}$	Drain-Source On-State-Resistance	V_{GS}=6V, I_D=3.9A	T_J=25°C		138	90	mΩ
			T_J=150°C		300		
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=400V, f=100kHz			96		pF
C_{oss}	Output Capacitance				30		
C_{rss}	Reverse Transfer Capacitance				0.5		
$C_{o(er)}$	Effective Output Capacitance Energy Related (6)	V_{GS}=0V, V_{DS}=0 to 400V			43		pF
$C_{o(tr)}$	Effective Output Capacitance Time Related (7)				60		
R_G	Gate Resistance	f=5MHz, open drain			5.8		Ω
SWITCHING							
Q_g	Gate Charge	V_{GS}=0 to 6V, V_{DS} =400V, I_D =3.9A			2.8		nC
Q_{gs}	Gate Source Charge				0.25		
Q_{gd}	Gate Drain Charge				1.1		
V_{plat}	Gate Plateau Voltage	V_{DS} = 400V, I_D =3.9A			2.2		V
Q_{oss}	Output Charge	V_{GS}=0V, V_{DS}=0 to 400V			24.5		nC
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400 V; ID = 8 A; L = 318 µH; V_{GS} = 6 V; Ron = 10 Ω; Roff = 2 Ω;			1.4		ns
$t_{d(off)}$	Turn-Off Delay Time				1.7		
t_r	Rise Time				4		
t_f	Fall Time				4		

Electrical Characteristics *(Continued)*

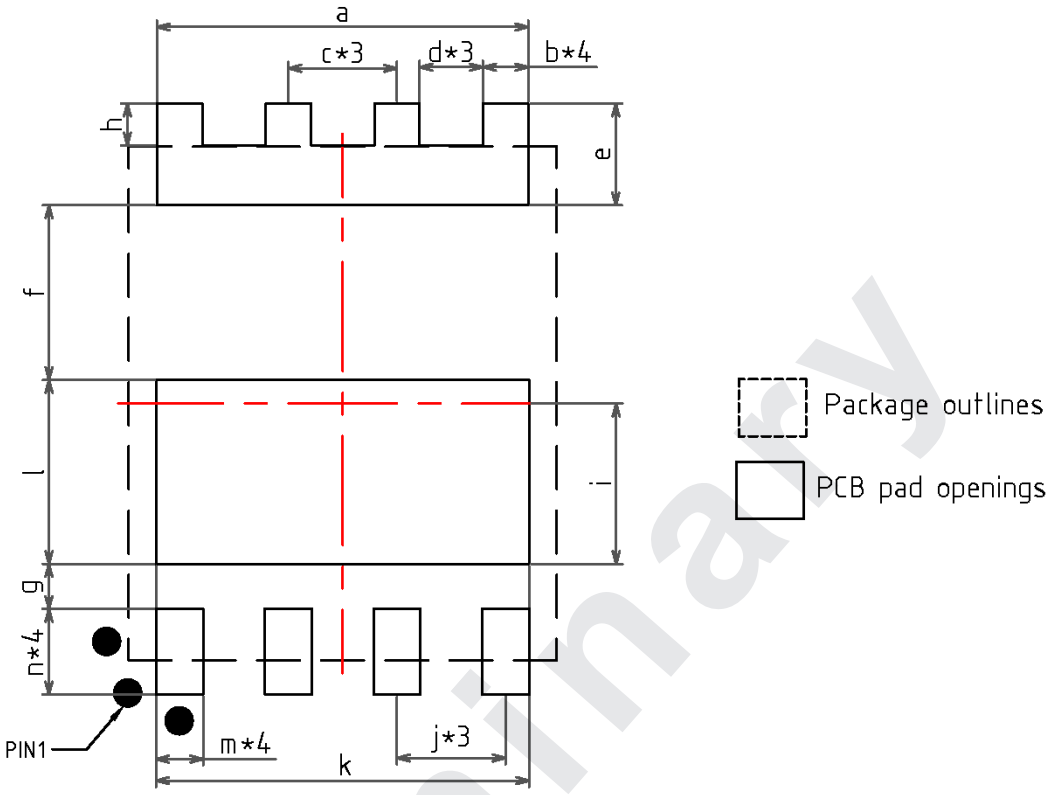
(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
REVERSE CONDUCTION							
V_{SD}	Source-Drain Reverse Voltage	V_{GS} = 0 V, I_S = 3.9A, T_J = 25°C			2.6		V
$I_{S,\ pulse}$	Reverse Pulsed Current	V_{GS} = 6 V, t_{pulse} = 10 µs				20.5	A
Q_{rr}	Reverse Recovery Charge	V_R = 400 V, I_S = 3.9A, dv/dt = 1 kA/ µs			0		nC
t_{rr}	Reverse Recovery Time				0		ns
I_{rrm}	Peak Reverse Recovery Current				0		A

Notes:

1. $V_{DS,transient}$ is intended for non-repetitive events, t_{PULSE} < 200 µs.
2. $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.
3. Limit was extracted from characterization test, not measured during production.
4. Power dissipation, and consequently max. current ratings are obtained using max. thermal resistance and max. temperature of 150°C.
5. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
6. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while VDS is rising from 0 to 400 V.
7. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while VDS is rising from 0 to 400 V.

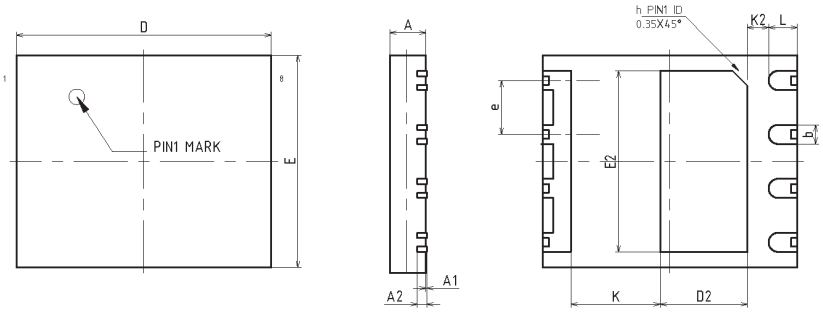
Recommended PCB Footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	4.340	h	0.490
b	0.530	i	1.875
c	1.270	j	1.270
d	0.740	k	4.360
e	1.190	l	2.150
f	2.040	m	0.550
g	0.525	n	1.000

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale

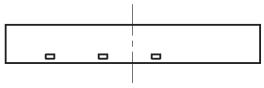
Package Dimensions, DFN5x6



Top view

Bottom view

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.40	0.45	0.50
D	5.90	6.00	6.10
D2	1.95	2.05	2.15
e		1.27	
E	4.90	5.00	5.10
E2	4.16	4.26	4.36
L	0.625	0.675	0.725
K		2.10REF	
K2		0.50REF	
h	0.30	0.35	0.40

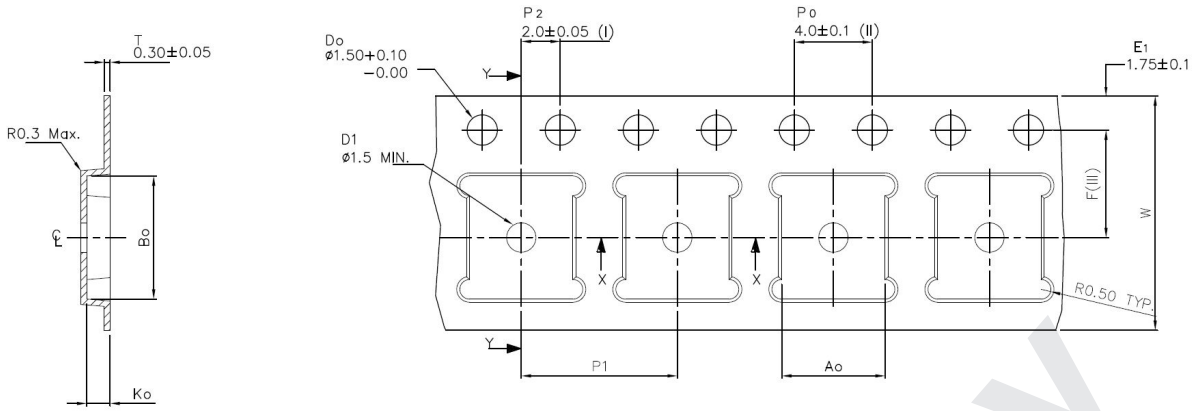


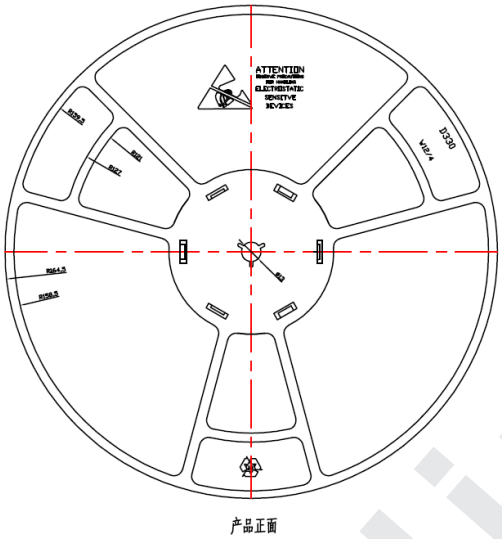
Side view

Notes:

1. Dimension and tolerance conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. Lead coplanarity will be 0.1 millimeters max.
4. Complies with JEDEC MO-229.
5. Drawing is not to scale.
6. Dimensions do not include mold protrusion.
7. Package outline exclusive of metal burr dimensions.

Tape and Reel Dimensions, DFN5x6





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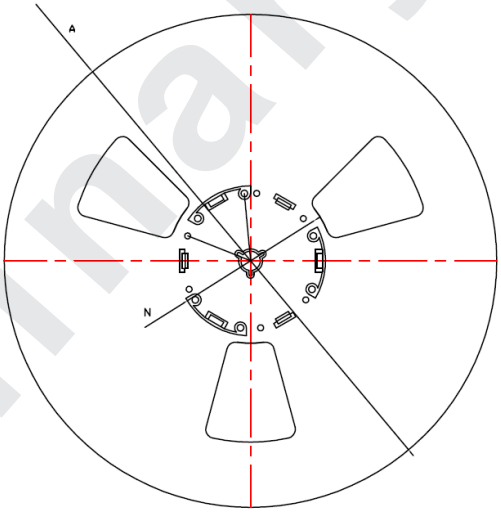
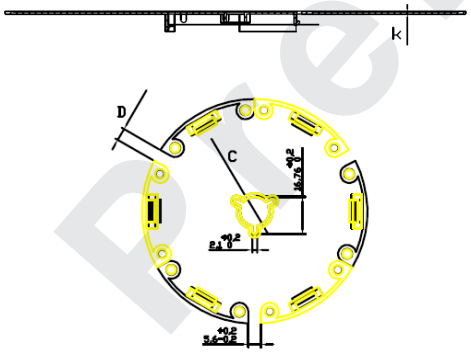
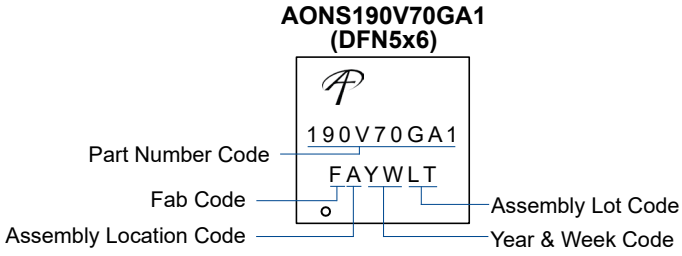




SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A_0	5.20	5.30	5.40
B_0	6.20	6.30	6.40
K_0	1.10	1.20	1.30
F	5.45	5.50	5.55
P1	7.90	8.00	8.10
W	11.70	12.00	12.30
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	12.40	12.40	14.40
w2	16.60	16.60	18.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

Part Marking



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