ALPHA & OMEGA SEMICONDUCTOR

AONS240V70GA1

700V GaN Enhancement-mode Power Transistor

Features

- 700V GaN enhancement-mode transistor
- Normally-off design
- No Qrr (reverse recovery charge)
- Low Qg (gate charge), low Qoss (output charge)
- Integrated ESD protection

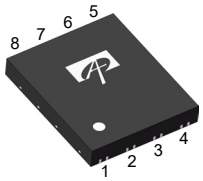
Applications

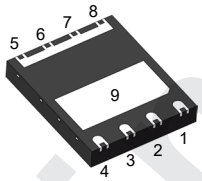
- AC/DC and DC/DC converters, totem pole PFC, fastbattery charging, high density and high efficiency power conversion

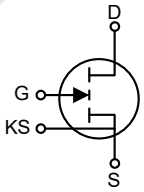
Product Summary at T_J = 25°C

$V_{DS, max}$	700V
$R_{DS(on), max}$ @ V_{GS} = 6V	240mΩ
$Q_{g, typ}$ @ V_{DS} = 400V	2nC
$I_{D, pulse}$	18A
Q_{oss} @ V_{DS} = 400V	21nC
Q_{rr} @ V_{DS} = 400V	0nC

Pin Configuration







Pin Information

Gate	Drain	Kelvin Source	Source
4	5, 6, 7, 8	3	1, 2, 9

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AONS240V70GA1	DFN5x6	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AONS240V70GA1	Units
$V_{DS, max}$	Drain Source Voltage	V_{GS} = 0V, T_J = -55°C to 150°C	700	V
$V_{DS, trans}$	Drain Source Voltage Transient (1)	V_{GS} = 0V	800	V
$V_{DS, pulse}$	Drain Source Voltage Pulsed (2)	T_C = 25°C, total time < 10 hours	750	V
		T_C = 125°C, total time < 1 hour		
I_D	Continuous Drain Current	T_C = 25°C	10	A
$I_{D, pulse}$	Pulsed Drain Current (3)	T_C = 25°C, V_{GS} = 6V, t_{pulse} = 10µs	18	A
		T_C = 125°C, V_{GS} = 6V, t_{pulse} = 10µs	10	A
V_{GS}	Gate Source Voltage, Continuous (4)	T_J = -55°C to 150°C	-6 to 7	V
$V_{GS, pulse}$	Gate Source Voltage, Pulsed	T_J = -55°C to 150°C, t_{pulse} = 50ns, f = 100kHz, open drain	-20 to 10	V
P_{tot}	Power Dissipation (5)	T_C = 25°C	75	W
$T_{j, stg}$	Junction and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Note	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (6)	70			°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	1.66			°C/W
T_{sold}	Maximum Reflow Soldering Temperature	260		MSL3	°C

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 11mA	T_J = 25°C	1.2	1.7	2.5	V
			T_J = 150°C		1.7		
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 700V, V_{GS} = 0V	T_J = 25°C		0.4	20	µA
			T_J = 150°C		5		
I_{GSS}	Gate-Source Leakage Current	V_{GS} = 6V, V_{DS} = 0V			50		µA
$R_{DS(on)}$	Drain-Source On-State-Resistance	V_G = 6V, I_D = 3A	T_J = 25°C		165	240	mΩ
			T_J = 150°C		360		
R_G	Gate Resistance	f = 5MHz, open drain			6		Ω
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 400V, f = 100kHz			79		pF
C_{oss}	Output Capacitance				25		
C_{rss}	Reverse Transfer Capacitance				0.2		
$C_{o(er)}$	Effective Output Capacitance Energy Related (7)	V_{GS} = 0V, V_{DS} = 0 to 400V			36		pF
$C_{o(tr)}$	Effective Output Capacitance Time Related (8)				52		
Q_{oss}	Output Charge	V_{GS} = 0V, V_{DS} = 0 to 400V			21		nC
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V; I_D = 6A; L = 318µH; V_{GS} = 6V; Ron = 10Ω; Roff = 2Ω; See Figure 22			2		ns
$t_{d(off)}$	Turn-Off Delay Time				4		
t_r	Rise Time				5		
t_f	Fall Time				6		
GATE CHARGE							
Q_G	Gate Charge	V_{GS} = 0 to 6V, V_{DS} = 400V, I_D = 3A			2		nC
Q_{GS}	Gate-Source Charge				0.2		
Q_{GD}	Gate-Drain Charge				0.7		
V_{Plat}	Gate Plateau Voltage	V_{DS} = 400V, I_D = 3A			2.5		V

Electrical Characteristics *(Continued)*

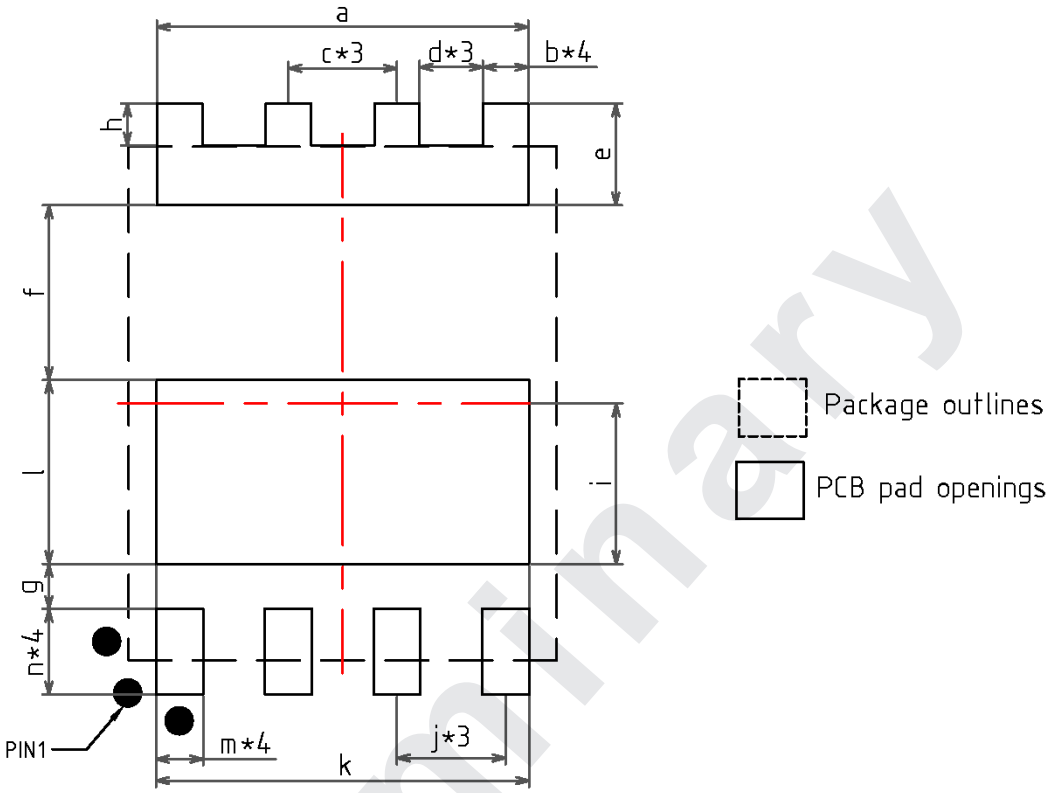
(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
REVERSE CONDUCTION							
V_{SD}	Source-Drain Reverse Voltage	V_{GS} = 0V, I_S = 3A			2.6		V
$I_{S,\ pulse}$	Reverse Pulsed Current	V_{GS} = 6V, t_{pulse} = 10µs				18	A
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400V, I_S = 3A			0		nC
t_{rr}	Reverse Recovery Time				0		ns
I_{rrm}	Peak Reverse Recovery Current				0		A

Notes:

1. $V_{DS,transient}$ is intended for non-repetitive events, t_{PULSE} < 200µs.
2. $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100ns.
3. Limit was extracted from characterization test, not measured during production.
4. The minimum V_{GS} clamped by ESD protection circuit, as shown in Figure 8.
5. Power dissipation, and consequently max. current ratings are obtained using max. thermal resistance and max. temperature of 150°C.
6. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
7. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while VDS is rising from 0 to 400V.
8. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while VDS is rising from 0 to 400V.

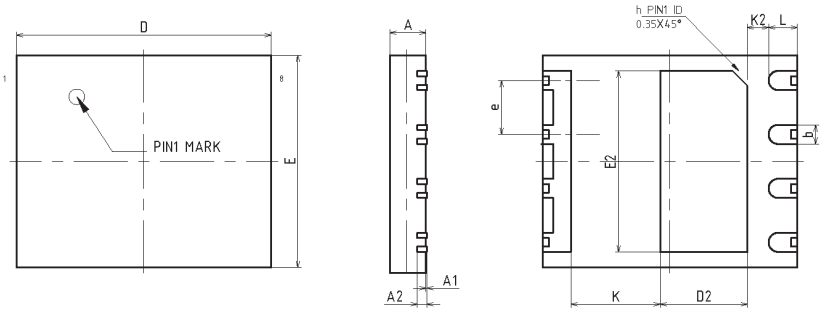
Recommended PCB Footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	4.340	h	0.490
b	0.530	i	1.875
c	1.270	j	1.270
d	0.740	k	4.360
e	1.190	l	2.150
f	2.040	m	0.550
g	0.525	n	1.000

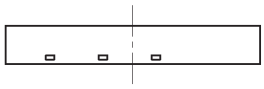
Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale

Package Dimensions, DFN5x6



Top view

Bottom view



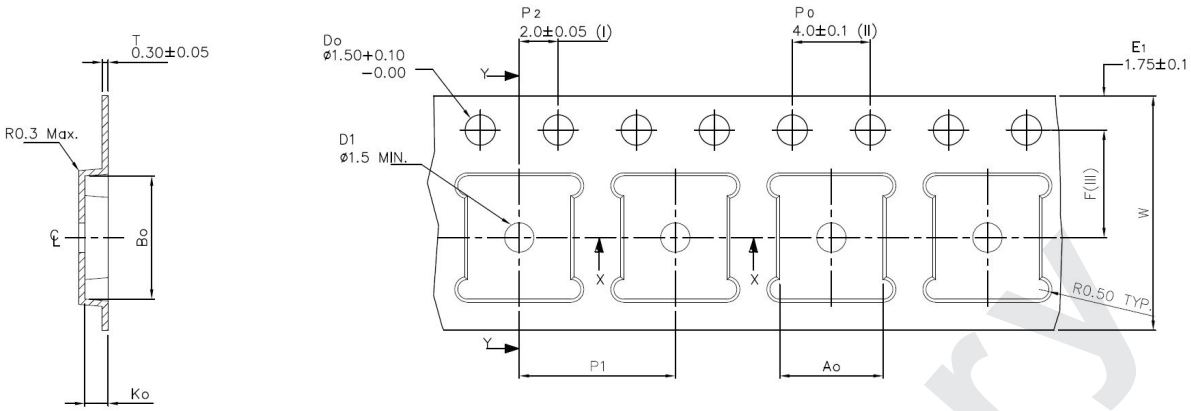
Side view

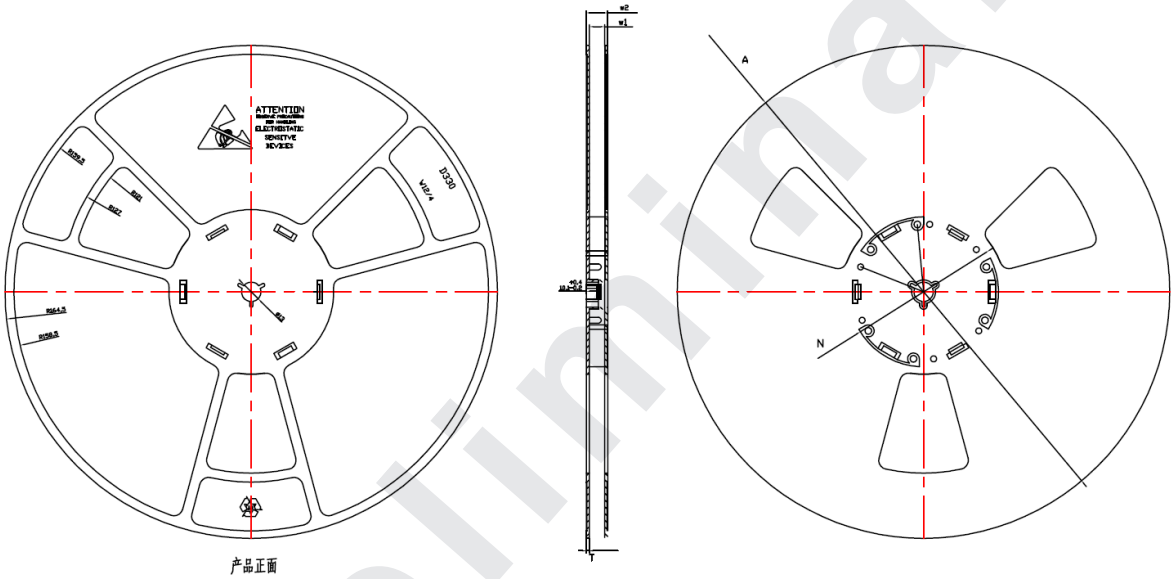
SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.40	0.45	0.50
D	5.90	6.00	6.10
D2	1.95	2.05	2.15
e		1.27	
E	4.90	5.00	5.10
E2	4.16	4.26	4.36
L	0.625	0.675	0.725
K		2.10REF	
K2		0.50REF	
h	0.30	0.35	0.40

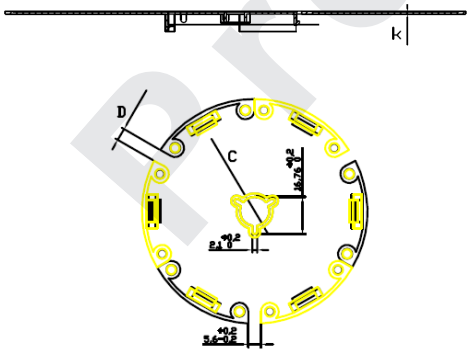
Notes:

1. Dimension and tolerance conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. Lead coplanarity will be 0.1 millimeters max.
4. Complies with JEDEC MO-229.
5. Drawing is not to scale.
6. Dimensions do not include mold protrusion.
7. Package outline exclusive of metal burr dimensions.

Tape and Reel Dimensions, DFN5x6







SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A_0	5.20	5.30	5.40
B_0	6.20	6.30	6.40
K_0	1.10	1.20	1.30
F	5.45	5.50	5.55
P1	7.90	8.00	8.10
W	11.70	12.00	12.30
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	12.40	12.40	14.40
w2	16.60	16.60	18.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.