ALPHA & OMEGA SEMICONDUCTOR

AONV080V65GA1

650V GaN Enhancement-mode Power Transistor

Features

- 650V GaN enhancement-mode transistor
- Normally-off design
- No Qrr (reverse recovery charge)
- Low Qg (gate charge), low Qoss (output charge)
- Integrated ESD protection

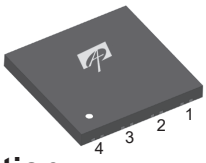
Applications

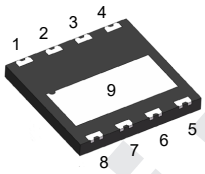
- AC/DC and DC/DC converters, BCM/DCM totem pole PFC, fast battery charging, high density and high efficiency power conversion

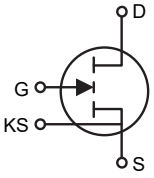
Product Summary at T_J = 25°C

$V_{DS, max}$	650V
$R_{DS(on), max}$ @ V_{GS} = 6V	80mΩ
$Q_{g, typ}$ @ V_{DS} = 400V	6.2nC
$I_{D, pulse}$	58A
Q_{oss} @ V_{DS} = 400V	60nC
Q_{rr} @ V_{DS} = 400V	0nC

Pin Configuration







Pin Information

Gate	Drain	Kelvin Source	Source
8	1, 2, 3, 4	7	5, 6, 9

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AONV080V65GA1	DFN8x8	Tape and Reel	1500

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AONV080V65GA1	Units
$V_{DS, max}$	Drain Source Voltage	V_{GS} = 0V, T_J = -55°C to 150°C	650	V
$V_{DS, trans}$	Drain Source Voltage Transient (1)	V_{GS} = 0V	800	
$V_{DS, pulse}$	Drain Source Voltage Pulsed (2)	T_J = 25°C, total time < 10 hours	750	
		T_J = 125°C, total time < 1 hour		
I_D	Continuous Drain Current	T_C = 25°C	29	A
$I_{D, pulse}$	Pulsed Drain Current (3)	T_C = 25°C, V_{GS} = 6V, t_{pulse} = 10µs	58	
		T_C = 125°C, V_{GS} = 6V, t_{pulse} = 10µs	29	
V_{GS}	Gate Source Voltage, Continuous (4)	T_J = -55°C to 150°C	-6 to 7	V
$V_{GS, pulse}$	Gate Source Voltage, Pulsed	T_J = -55°C to 150°C, t_{pulse} = 50ns, f = 100kHz, open drain	-20 to 10	V
P_{tot}	Power Dissipation (5)	T_C = 25°C	188	W
$T_{j, stg}$	Operating and Storage Temperature		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Note	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (6)	33.6			°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	0.52			°C/W
T_{sold}	Maximum Reflow Soldering Temperature	260		MSL3	°C

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 30.7mA	T_J = 25°C	1.2	1.7	2.5	V
			T_J = 150°C		1.6		
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 650V, V_{GS} = 0V	T_J = 25°C		5	65	µA
			T_J = 150°C		13	390	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = 6V, V_{DS} = 0V			163		µA
$R_{DS(on)}$	Drain-Source On-State-Resistance	V_{GS} = 6V, I_D = 8A	T_J = 25°C		60	80	mΩ
			T_J = 150°C		135		
R_G	Gate Resistance	f = 5 MHz; open drain			3		Ω
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 400V, f = 100kHz			225		pF
C_{oss}	Output Capacitance				70		
C_{rss}	Reverse Transfer Capacitance				0.5		
$C_{o(er)}$	Effective Output Capacitance Energy Related (7)	V_{GS} = 0V, V_{DS} = 0 to 400V			105		pF
$C_{o(tr)}$	Effective Output Capacitance Time Related (8)				150		
Q_{oss}	Output Charge				60		nC
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V, I_D = 16A, L = 318µH, V_{GS} = 6V, R_{on} = 10Ω, R_{off} = 2Ω, See Figure 20			3		ns
$t_{d(off)}$	Turn-Off Delay Time				5		
t_r	Rise Time				4		
t_f	Fall Time				4		
GATE CHARGE							
Q_G	Gate Charge	V_{GS} = 0 to 6V, V_{DS} = 400V, I_D = 8A			6.2		nC
Q_{GS}	Gate-Source Charge				0.5		
Q_{GD}	Gate-Drain Charge				2.2		
V_{Plat}	Gate Plateau Voltage	V_{DS} = 400V, I_D = 8A			2.2		V

Electrical Characteristics *(Continued)*

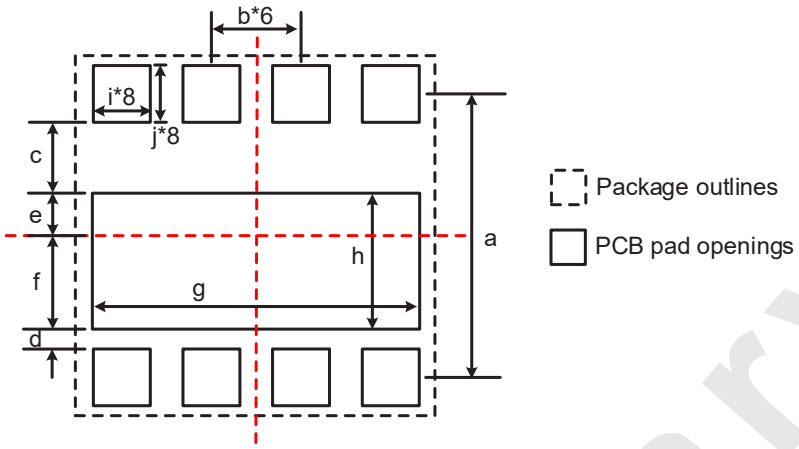
(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
REVERSE CONDUCTION							
V_{SD}	Source-Drain Reverse Voltage	V_{GS} = 0V, I_S = 8A			2.3		V
$I_{S,\ pulse}$	Reverse Pulsed Current	V_{GS} = 6V, t_{pulse} = 10µs				58	A
Q_{rr}	Reverse Recovery Charge	I_S = 8A, V_{DS} = 400V			0		nC
t_{rr}	Reverse Recovery Time				0		ns
I_{rrm}	Peak Reverse Recovery Current				0		A

Notes:

1. $V_{DS,transient}$ is intended for non-repetitive events, t_{PULSE} < 200µs.
2. $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100ns.
3. Limit was extracted from characterization test, not measured during production.
4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.
5. Power dissipation, and consequently max. current ratings are obtained using max. thermal resistance and max. temperature of 150°C.
6. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
7. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while VDS is rising from 0 to 400V.
8. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while VDS is rising from 0 to 400V.

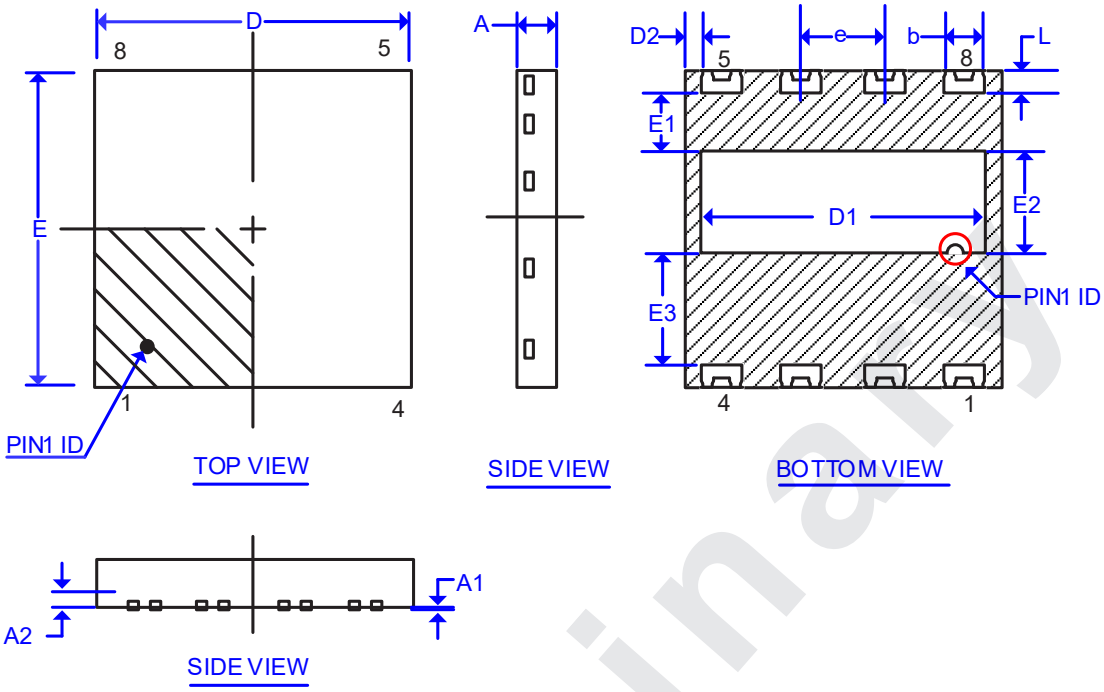
Recommended PCB Footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	7.800	f	2.750
b	2.000	g	7.500
c	2.325	h	3.700
d	0.525	i	1.400
e	0.950	j	1.250

Notes:
(1) All dimension are in millimeters.
(2) Drawing is not to scale.

Package Dimensions, DFN8x8

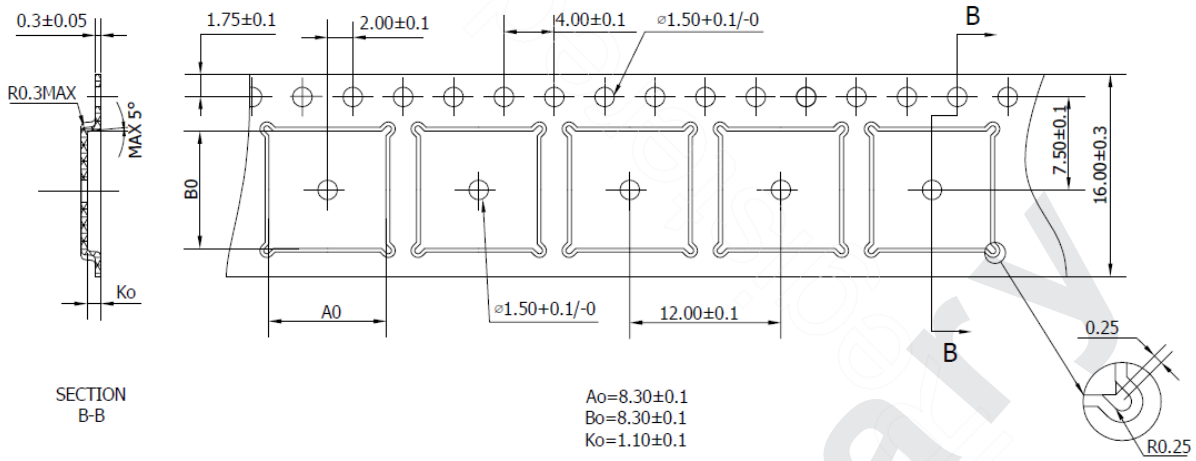


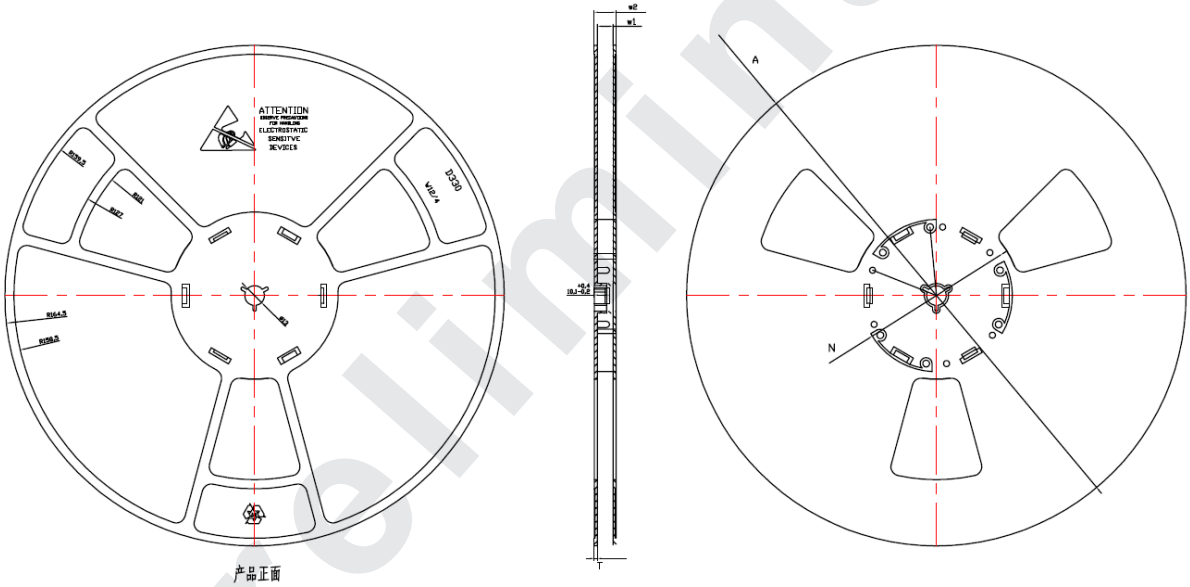
SYMBOL	DIMENSION			SYMBOL	DIMENSION		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.90	1.00	E	8.00 B.S.C		
A1	0.00	0.02	0.05	E1	0.90	1.00	1.10
A2	---	0.203 ref	---	E2	3.10	3.20	3.30
b	0.92	1.00	1.05	E3	2.70	2.80	2.90
D	8.00 B.S.C			e	2.00 B.S.C		
D1	6.84	6.94	7.04	L	0.40	0.50	0.60
D2	0.40	0.50	0.60				

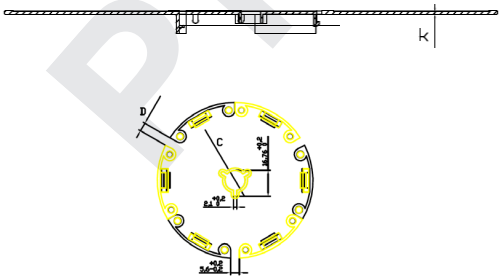
Notes:

(1) Dimension and tolerance conform to ASME Y14.5-2009.
(2) All dimension are in millimeters.
(3) Lead coplanarity shall be 0.1 millimeters max.
(4) Complies with JEDEC MO-229.
(5) Drawing is not to scale.
(6) Dimensions do not include mold protrusion.
(7) Package outline exclusive of metal burr dimensions.

Tape and Reel Dimensions, DFN8x8







SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	16.40	16.40	18.40
w2	20.60	20.60	22.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

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