

AOSE018V10GA1

100V GaN Enhancement-mode

100V

1.8mΩ

Power Transistor

Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

Applications

- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver

Pin Configuration



Pin Information

Top View

Pin	Pin Description	Pin Function
1, 2, 25	Gate	Driver Gate
3-7, 9, 11, 21, 23	Source	Source
8, 10, 12-20, 22, 24	Drain	Power Drain

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity	
AOSE018V10GA1	En-FCQFN 4x6	Tape and Reel	1500	

Contact local sales office for full product datasheet.

V _{DS,} max	
$R_{DS(on),}$ max @ V_{GS} = 6V	

Q _{g, typ} @ V _{DS} = 50 V	22nC
I _{D, pulse}	60A
Q _{OSS} @ V _{DS} = 50 V	320 nC
Q _{rr} @ V _{DS} = 50V	125nC

Product Summary at T_J = 25°C





Absolute Maximum Ratings (T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Max	Units
V _{DS}	Drain-to-Source Voltage (Continuous)	100	V
V _{DS(tr)}	Drain-to-Source Voltage (up to 300,000 5ms pulse at 150°C)	120	V
1	Continuous Current ($T_A = 25^{\circ}C$)	100	А
'D	Pulsed ($T_A = 25^{\circ}C$, $T_{Pulse} = 100 \mu s$)	320	А
V	Gate-to-Source Voltage	6	V
*GS	Gate-to-Source Voltage	-4	V
Tj	Operating Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-40 to 150	°C

Thermal Characteristics

Symbol	Parameter	Тур	Note	Units
R _{θJC}	Thermal Resistance Junction-to-Case	0.24	-	°C/W
R _{θJB}	Thermal Resistance Junction-to-Board	1.31	-	°C/W
R _{eja}	Thermal Resistance, Junction to Ambient ⁽¹⁾	56.63	-	°C/W
T _{sold}	Maximum Reflow Soldering Temperature	260	MSL3	°C

Note:

1. R_{BJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Electrical Characteristics

$(T_1 = 25^{\circ}C, unless otherwise noted)$

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Static Characteristics						
B _{VDSS}	Drain-to-Source Voltage	V _{GS} = 0V, I _D = 900µA	100	-	-	V
I _{DSS}	Drain Source Leakage	V _{GS} = 0V, V _{DS} = 80V	-	9.5	93	μA
1	Gate-to-Source Forward Leakage	V _{GS} = 5V	-	2.8	55	μA
'GSS	Gate-to-Source Reverse Leakage	$V_{GS} = -4V$	-	0.3	1.2	μA
V _{GS(TH)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 21mA$	0.8	1.1	2.5	V
R _{DS(ON)}	Drain-Source On-state Resistance	V _{GS} = 5V, I _D = 40A	-	1.4	1.8	mΩ
V _{SD}	Source-Drain Forward Voltage	I _S = 0.5A, V _{GS} = 0V	-	1.5	-	V
Dynamic C	haracteristics					
C _{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 50V$	-	2500	-	
C _{OSS}	Output Capacitance	V _{GS} = 0V, V _{DS} = 50V	-	1100	-	
C _{RSS}	Reverse Transfer Capacitance	V _{GS} = 0V, V _{DS} = 50V	-	19	-	pF
C _{OSS(ER)}	Energy Related COSS	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 50V$	-	1700	-	
C _{OSS(TR)}	Time Related COSS	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 50V$	-	2500	-	
R _G	Gate Resistance	f = 5 MHz, open drain	-	1.8	-	Ω
Q _G	Total Gate Charge	V _{GS} = 5V, V _{DS} = 50V, I _D = 40A	-	22	-	
Q _{GS}	Gate to Source Charge	V _{DS} = 50V, I _D = 40A	-	4.5	-	
Q _{GD}	Gate to Drain Charge	V _{DS} = 50V, I _D = 40A	-	4.5	-	nC
Q _{G(TH)}	Gate Charge at Threshold	V _{DS} = 50V, I _D = 40A	-	2.5	-	1
Q _{OSS}	Output Charge	V _{GS} = 0V, V _{DS} = 50V	-	125	-	1



Recommended PCB Footprint



Recommended Stencil Drawing



SYMBOL	MILLIMETER	NOTE
С	4.56	5X
D1	0.21	3X
E1	0.21	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L1	0.21	4X
R2	2.46	
Q2	1.46	
S	2.6	



Package Dimensions, QFN4x6-25L



TOP VIEW



SIDE VIEW

> NOTE: 1)ALL DIMENSION ARE IN MILLIMETERS. 2)BOTTOM VIEW IS FT TESTER SIDE VIEW. 3)LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX. 4)COMPLIES WITH JEDEC MO-220. 5)DRAWING IS NOT TO SCALE. 6)BOTTOM LEAD SURFACE FINISH IS SN.

CVMPOL	MILLIMETER			NOTE
STIVIBUL	MIN	NOM	MAX	NOTE
Α	3.9	4.0	4.1	
В	5.9	6.0	6.1	
D	0.20	0.25	0.30	3X
E	0.20	0.25	0.30	13X
F		2X		
G	0.5 BASIC			10X
Н	0.2 REF			3X
К		1.07 BASIC		
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
U	0.45 REF			2X
Z	0.203 REF			
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	

Rev. 1.0 July 2025

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Tape and Reel Dimensions, QFN4x6-25L





Part Marking



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