ALPHA & OMEGA SEMICONDUCTOR

AOTL070V65GA1

650V GaN Enhancement-mode Power Transistor

Features

- 650V GaN enhancement-mode transistor
- Normally-off design
- No Qrr (reverse recovery charge)
- Low Qg (gate charge), low Qoss (output charge)
- Integrated ESD protection

Applications

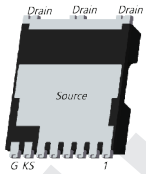
- PFC and PWM stages (LLC, FSFB, TTF) of Server, Telecom, Industrial, UPS, and Solar Inverters

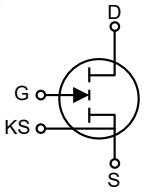
Product Summary at T_J = 25°C

$V_{DS, max}$	650V
$R_{DS(on), max}$ @ V_{GS} = 6V	70mΩ
$Q_{g, typ}$ @ V_{DS} = 400V	8.5nC
$I_{D, pulse}$	60A
Q_{oss} @ V_{DS} = 400V	94.7nC
Q_{rr} @ V_{DS} = 400V	0nC

RoHS Compliant

Pin Configuration





Pin Information

Gate	Drain	Kelvin Source	Source
8	9, 10, 11	7	1, 2, 3, 4, 5, 6

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AOTL070V65GA1	TOLL	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AOTL070V65GA1	Units
$V_{DS, max}$	Drain Source Voltage	V_{GS}=0V, T_J=-55°C to 150°C	650	V
$V_{DS, trans}$	Drain Source Voltage Transient (1)	V_{GS}=0V	800	
$V_{DS, pulse}$	Drain Source Voltage Pulsed (2)	T_C=25°C, total time < 10 hours	750	
		T_C=125°C, total time < 1 hour		
I_D	Continuous Drain Current	T_C=25°C	26	A
		T_C=125°C	17	
$I_{D, pulse}$	Pulsed Drain Current (3)	T_C=25°C, V_{GS}=6V, t_{pulse}=10µs	60	
		T_C=125°C, V_{GS}=6V, t_{pulse}=10µs	31	
V_{GS}	Gate Source Voltage, Continuous	T_J=-55°C to 150°C	-6 to 7	V
$V_{GS, pulse}$	Gate Source Voltage, Pulsed	T_J=-55°C to 150°C, t_{pulse}=50ns, f = 100kHz, open drain	-20 to 10	V
P_{tot}	Power Dissipation (4)	T_C=25°C	231	W
$T_{j, stg}$	Junction and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Note	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (5)	56.5			°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	0.54	0.65		°C/W
T_{sold}	Maximum Reflow Soldering Temperature	260		MSL3	°C

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, I_D=40mA	T_J=25°C	1.2	1.7	2.5	V
			T_J=150°C		1.6		
I_{DSS}	Drain-Source Leakage Current	V_{DS}=650V, V_{GS}=0V	T_J=25°C		1	65	µA
			T_J=150°C		10		
I_{GSS}	Gate-Source Leakage Current	V_{GS}=6V, V_{DS}=0V, T_J=25°C			110		µA
$R_{DS(on)}$	Drain-Source On-State-Resistance	V_{GS}=6V, I_D=10A	T_J=25°C		53	70	mΩ
			T_J=150°C		122		
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=400V, f=100kHz			300		pF
C_{oss}	Output Capacitance				135		
C_{rss}	Reverse Transfer Capacitance				2.3		
$C_{o(er)}$	Effective Output Capacitance Energy Related (6)	V_{GS}=0V, V_{DS}=0 to 400V			190		pF
$C_{o(tr)}$	Effective Output Capacitance Time Related (7)				240		
R_G	Gate Resistance	f=5MHz, open drain			1.4		Ω
SWITCHING							
Q_G	Gate Charge	V_{GS}=0 to 6V, V_{DS} =400V, I_D =10A			8.5		nC
Q_{GS}	Gate Source Charge				0.7		
Q_{GD}	Gate Drain Charge				3.6		
V_{plat}	Gate Plateau Voltage	V_{DS} = 400V, I_D =10A			2.3		V
Q_{oss}	Output Charge	V_{GS}=0V, V_{DS}=0 to 400V			94.7		nC
$t_{d(on)}$	Turn-On Delay Time	V_{DS}= 400V, I_D=10A, $L_{parasitic}$ = 8nH, V_{GS}=6V, R_{on}=10Ω, R_{off}=2Ω, L=350µH, Lp = 8nH FWD: AOTL070V65GA1			10		ns
$t_{d(off)}$	Turn-Off Delay Time				7		
t_r	Rise Time				9		
t_f	Fall Time				9		

Electrical Characteristics *(Continued)*

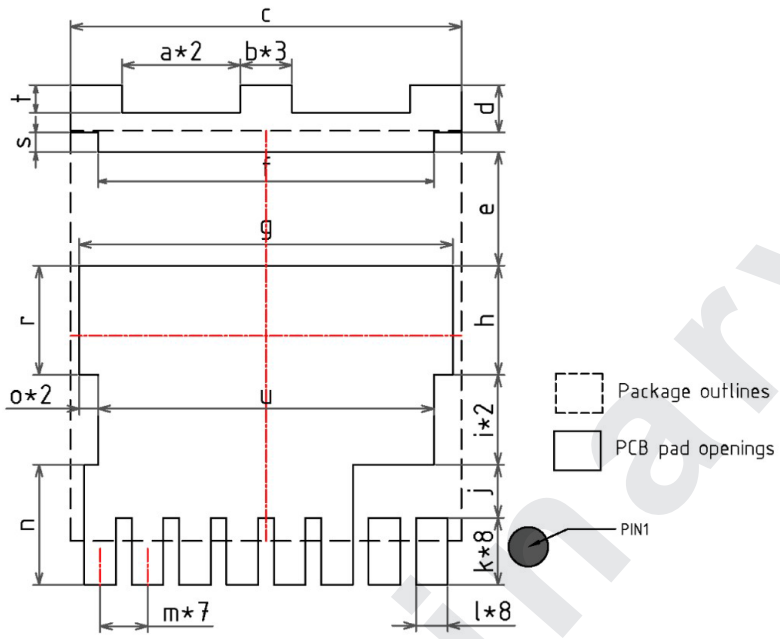
(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
REVERSE CONDUCTION						
V_{SD}	Source-Drain Reverse Voltage	V_{GS} = 0V, I_S = 10A, T_J = 25°C		2.4		V
$I_{S,\ pulse}$	Reverse Pulsed Current	V_{GS} = 6V, t_{pulse} = 10µs			58	A
Q_{rr}	Reverse Recovery Charge	V_R = 400V, I_S = 10A, dv/dt = 1kA/ µs		0		nC
t_{rr}	Reverse Recovery Time			0		ns
I_{rrm}	Peak Reverse Recovery Current			0		A

Notes:

1. $V_{DS,transient}$ is intended for non-repetitive events, t_{PULSE} < 200µs.
2. $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100ns.
3. Limit was extracted from characterization test, not measured during production.
4. Power dissipation, and consequently max. current ratings are obtained using max. thermal resistance and max. temperature of 150°C.
5. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
6. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while VDS is rising from 0 to 400 V.
7. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while VDS is rising from 0 to 400 V.

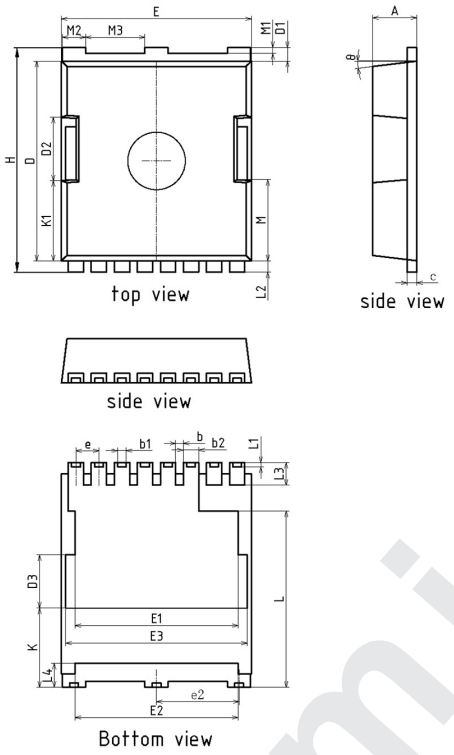
Recommended PCB Footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	3.00	k	1.70
b	1.30	l	0.80
c	9.90	m	1.20
d	1.20	n	3.05
e	2.88	o	0.48
f	8.50	r	2.77
g	9.46	s	0.50
h	2.77	t	0.70
i	2.28	u	8.50
j	1.35	/	/

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

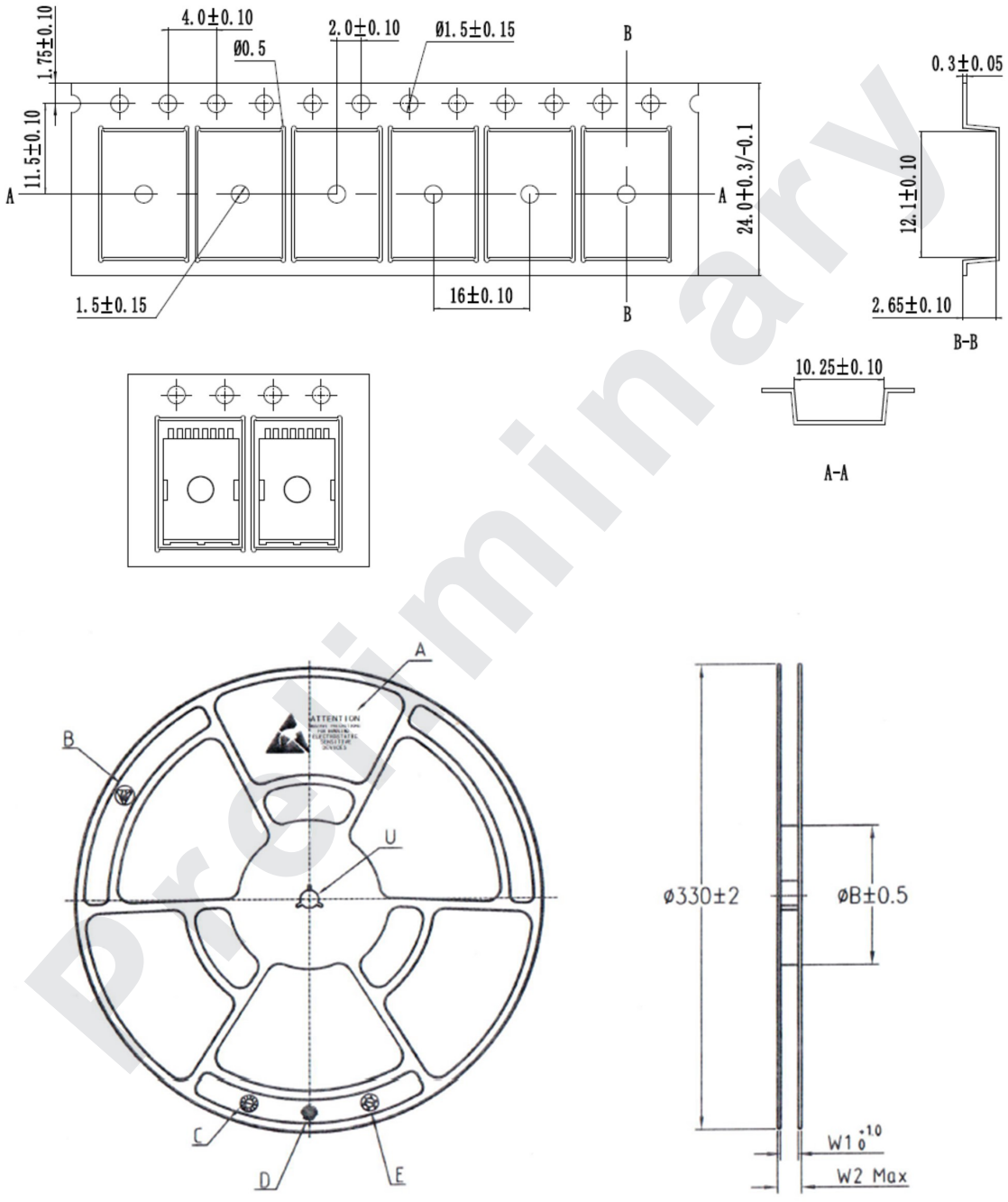
Package Dimensions, TOLL



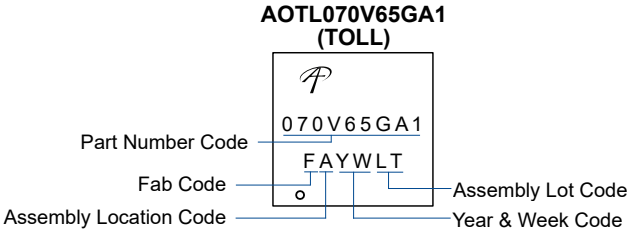
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.30	0.40	0.50
b1	0.31	0.43	0.55
b2	0.65	0.80	0.90
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2		3.30REF	
D3		2.77REF	
E	9.70	9.90	10.10
E1		8.50REF	
E2		8.50REF	
E3		9.46REF	
e	1.10	1.20	1.30
H	11.48	11.68	11.88
K		4.08REF	
K1		4.18REF	
L		9.13REF	
L1		0.23REF	
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	1.00	1.20	1.40
M		4.18REF	
M1		0.26REF	
M2	1.10	1.20	1.30
M3		3.10REF	
Θ		10.00REF	
e2	4.20	4.30	4.40

Notes:
(1) Dimensioning and toleranceing confirm to ASME Y14.5M-1994
(2) All dimensions are in millimeters, angles are in degrees
(3) Coplanarity applies to the exposed heat slug as well as the terminal
(4) Radius on terminal is optional
(5) General tolerance: ± 0.10 mm

Tape and Reel Dimensions, TOLL



Part Marking



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