

# ***Alpha & Omega Semiconductor Product Reliability Qualification Report***

**AONC68816** rev A

**ALPHA & OMEGA Semiconductor, Inc**

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This report delineates the product's quality and reliability test outcomes. Specific sample sizes undergo accelerated environmental tests, with corresponding electrical testing before and after each interval. Analysis of the conclusive electrical test results affirms the product's adherence to AOS quality and reliability standards in accordance with **JEDEC**. Reference to the existing qualification outcomes for similar products is warranted due to structural similarities. The released product will be classified by its process family and undergo regular monitoring to ensure continual enhancements in product quality.

## I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Duration	Lots/SS	Number of Failures	Reference Standard
<b>HTGB</b> <i>High Temperature Gate Bias</i>	175°C Vgs=100% of Vgsmax	1000 hrs	3 * 77	0/231	JESD22-A108
<b>HTRB</b> <i>High Temperature Reverse Bias</i>	175°C Vds=100% of Vdsmax	1000 hrs	3 * 77	0/231	JESD22-A108
<b>PC</b> <i>Precondition</i>	168 hrs, 85°C, 85%RH, 3 cycles reflow @ 260°C (MSL 1)	-	18 * 77	0/1386	JESD22-A113 J-STD-020
<b>HAST*</b> <i>Highly Accelerated Stress Test</i>	130°C, 85%RH, Vds = 80% of Vdsmax up to 42V	96 hrs	3 * 77	0/231	JESD22-A110
<b>H3TRB*</b> <i>High Humidity High Temperature Reverse Bias</i>	85°C, 85%RH, Vds = 80% of Vdsmax up to 100V	1000 hrs	3 * 77	0/231	JESD22-A101
<b>AC*</b> <i>Autoclave</i>	121°C, 100%RH, 15psig	96 hrs	3 * 77	0/231	JESD22-A102
<b>TC*</b> <i>Temperature Cycling</i>	-55°C to 150°C, air to air	1000 cycles	3 * 77	0/231	JESD22-A104
<b>HTSL*</b> <i>High Temperature Storage Life</i>	175°C	1000 hrs	3 * 77	0/231	JESD22-A103
<b>IOL*</b> <i>Intermittent Operational Life</i>	$\Delta T_j = 100^\circ\text{C}$ $t_{on} = 2 \text{ minutes}$ $t_{off} = 2 \text{ minutes}$	15000 cycles	3 * 77	0/231	MIL-STD-750 Method 1037
<b>ESD_HBM</b>	Class 1B (500V to <1000V)	-	3 pcs	-	JS-001
<b>ESD_CDM</b>	Class C3 (≥1000V)	-	3 pcs	-	JS-002

### Notes:

\* For SMD devices reliability stress tests performed after PC (precondition).

## II. Reliability Evaluation

**FIT rate (per billion): 2.61**

**MTTF = 43670 years**

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

At 60% Confidence Level

**Failure Rate** =  $\text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 2.61$

**MTTF** =  $10^9 / \text{FIT} = 43670$  years

**Chi<sup>2</sup>** = Chi Squared Distribution, determined by the number of failures and confidence interval

**N** = Total Number of units from burn-in tests

**H** = Duration of burn-in testing

**Af** = Acceleration Factor from Test to Use Conditions ( $E_a = 0.7\text{eV}$  and  $T_{J u} = 55^\circ\text{C}$ )

Acceleration Factor [**Af**] = **Exp** [ $E_a / k (1/T_{J u} - 1/T_{J s})$ ]

**Acceleration Factor ratio list:**

	55 deg C	70 deg C	85 deg C	100 deg C	125 deg C	150 deg C	175 deg C
<b>Af</b>	758	256	95	38	9.7	2.9	1

**T<sub>J s</sub>** = Stressed junction temperature in degree (Kelvin),  $K = C + 273.16$

**T<sub>J u</sub>** = The use junction temperature in degree (Kelvin),  $K = C + 273.16$

**k** = Boltzmann's constant,  $8.617164 \times 10^{-5} \text{eV} / K$