Alpha & Omega Semiconductor Product Reliability Qualification Report

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ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

This report delineates the product's quality and reliability test outcomes. Specific sample sizes undergo accelerated environmental tests, with corresponding electrical testing before and after each interval. Analysis of the conclusive electrical test results affirms the product's adherence to AOS quality and reliability standards in accordance with **JEDEC**. Reference to the existing qualification outcomes for similar products is warranted due to structural similarities. The released product will be classified by its process family and undergo regular monitoring to ensure continual enhancements in product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Duration	Lots/SS	Number of Failures	Reference Standard
HTGB *High Temperature Gate Bias*	**175°C Vgs=100% of Vgsmax**	**1000 hrs**	**3 * 77**	**0/231**	**JESD22-A108**
HTRB *High Temperature Reverse Bias*	**175°C Vds=100% of Vdsmax**	**1000 hrs**	**3 * 77**	**0/231**	**JESD22-A108**
PC *Precondition*	**168 hrs, 85°C, 85%RH, 3 cycles reflow @ 260°C (MSL 1)**	**-**	**18 * 77**	**0/1386**	**JESD22-A113 J-STD-020**
HAST* *Highly Accelerated Stress Test*	**130°C, 85%RH, Vds = 80% of Vdsmax up to 42V**	**96 hrs**	**3 * 77**	**0/231**	**JESD22-A110**
H3TRB* *High Humidity High Temperature Reverse Bias*	**85°C, 85%RH, Vds = 80% of Vdsmax up to 100V**	**1000 hrs**	**3 * 77**	**0/231**	**JESD22-A101**
AC* *Autoclave*	**121°C, 100%RH, 15psig**	**96 hrs**	**3 * 77**	**0/231**	**JESD22-A102**
TC* *Temperature Cycling*	**-65°C to 150°C, air to air**	**1000 cycles**	**3 * 77**	**0/231**	**JESD22-A104**
HTSL* *High Temperature Storage Life*	**175°C**	**1000 hrs**	**3 * 77**	**0/231**	**JESD22-A103**
IOL* *Intermittent Operational Life*	**ΔTj = 100°C t_{on} = 2 minutes t_{off} = 2 minutes**	**15000 cycles**	**3 * 77**	**0/231**	**MIL-STD-750 Method 1037**
ESD_HBM	**Class 1C (1000V to <2000V)**	**-**	**3 pcs**	**-**	**JS-001**
ESD_CDM	**Class C3 (≥1000V)**	**-**	**3 pcs**	**-**	**JS-002**

Notes:
* For SMD devices reliability stress tests performed after PC (precondition).

II. Reliability Evaluation

FIT rate (per billion): 2.61
MTTF = 43670 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

At 60% Confidence Level
Failure Rate = $\text{Chi}^2 \times 10^9$ **/** **[**2 (N) (H) (Af)**] =** 2.61
MTTF = 10^9 / FIT = 43670 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and T_J u = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/T_J u – 1/T_J s)]

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	125 deg C	150 deg C	175 deg C
Af	**758**	**256**	**95**	**38**	**9.7**	**2.9**	**1**

T_J s = Stressed junction temperature in degree (Kelvin), K = C + 273.16
T_J u =The use junction temperature in degree (Kelvin), K = C + 273.16
k = Boltzmann’s constant, 8.617164 X 10^{-5}eV / K