ALPHA & OMEGA SEMICONDUCTOR

AOS Semiconductor Reliability Report

HVMOS Family Report, rev A

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This report applies for high voltage (900V/700V/650V/600V/500V) products assembled in following packages TO220 (F)/TO262 (F)/TO263/TO252 /TO251 (A).

"Commitment to Excellence at Quality & Reliability!"

To achieve this vision, AOS continuously strive for the excellence in design, manufacturing, reliability and proactively response to the customer's feedback.

AOS ensures that all the product quality and reliability exceed the customer's expectation by constantly assessing any potential risk, identifying cause of the suspected failures, driving corrective actions and developing prevention plan within the committed time through the continuously improvement.

This AOS product reliability report summarizes AOS Product Reliability result. The published product reliability data combines the results from new product Qualification Test Plan and routine Reliability Program activities. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. The released product will be categorized by the process family and be monitored on a quarterly basis for continuously improving the product quality. Table 1 lists the generic reliability qualification requirements and conditions:

Table 1: AOS Generic Reliability Qualification Requirements

Test Item	Test Condition	Time Point	Sample size	Acc/Reject
HTGB	Temp = 150°c , Vgs=100% of Vgsmax	168 / 500 hrs 1000 hrs	77 pcs / lot	0/1
HTRB	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 hrs 1000 hrs	77 pcs / lot	0/1
Solder reflow precondition	168hr 85°c /85%RH + 3 cycle reflow @250°c (MSL level 1)	-	The sum of PCT ,TC and HAST	0/1
HAST	130 +/- 2°C , 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	55 pcs / lot	0/1
Pressure Pot	121°C , 29.7psi, 100%RH	96 hrs	77 pcs / lot	0/1
Temperature Cycle	-65°C to 150°C, air to air,	250 / 500 cycles	77 pcs / lot	0/1
Power Cycle	Δ Tj = 125 °C	4286 cycles	77 pcs / lot	0/1

High Temperature Gate Bias (HTGB) & High Temperature Reverse Bias (HTRB)

HTGB burn-in stress is used to stress gate oxide at the elevated temperature environment hence any of the gate oxide integrity issue can be identified. HTRB burn-in stress is used to verify junction degradation under the maximum operation temperature.

Through HTGB & HTRB B/I stress test, the device lifetime in field operation & long term device level reliability can be determined. FIT rate is calculated by applying the Arrhenius equation with the activation energy of 0.7Ev and 60% of upper confidence level at 55 deg C operating conditions.

Solder reflow precondition (pre-con)

Solder reflow precondition is the test that simulates shipment and storage of package in under uncontrollable environment. Precondition is the pre-requirement for the mechanical related reliability tests (such as Temperature Cycle, Pressure Pot and High Acceleration Stress TEST (HAST). The routine of the test are: parts will be soaked in moisture then bake in pressure pot, or being placed into 85% RH, 85 deg C environment for 168 hrs. Then they will be run through a solder reflow oven with temperature at 260ºC+/- 5ºC or 250ºC+/- 5ºC (depending on package thickness and volume). The test condition totally complies with MSL level 1. Pre-condition is a test that is detected package delamination, lifted bond wire issue.

Temperature Cycling (TC)

Temperature cycling test is to evaluate the mechanical integrity of the package and the interaction between the die and the package. This is an air to air test at temperature range from -65ºC/150ºC and stress duration is from 250 cycles to 500 cycles.

Pressure Pot (PCT)

PCT test is the test that measures the ability of the device withstand to moisture and contaminant environment. The test is done under enclosed chamber with the condition 121ºC 15+/- 1PSIG, 100%RH and stress duration is 96 hrs.

High Acceleration Stress Test (HAST)

High acceleration stress test is to stress the devices under high humidity, high pressure environment under DC bias condition. If ionic contamination involved, the corrosion from metal layer can be accelerated by the HAST stress condition.

Power Cycle

The power cycle test is performed to determine that the ability of a device to withstand alternate exposures at high and low junction temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst case conditions encountered in typical application.

The following tables summarize the qualification results based on the device/process families and the package types, respectively.

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Summary of AOS High Voltage MOSFET product with TO220 (F)/TO262 (F)/TO263/TO252 /TO251 (A) package Qualification Results

Table 2 Product Family

Voltage	Device No.	Package
900V	AOTFXXN90	TO220F
700V	AOTFXXN70	TO220F
	AOTXXN70	TO220
650V	AOTFXXN65	TO220F
	AOTXXN65	TO220
	AOWFXXN65	TO262F
	AOWXXN65	TO262
600V	AOTFXXN60	TO-220F
	AOTXXN60	TO-220
	AOWFXXN60	TO262F
	AOWXXN60	TO262
	AOBXXN60(L)	TO263
	AODXXN60	TO252
	AOUXXN60	TO251
	AOIXXN60	TO251A
500V	AOWFXXN50	TO262F
	AOWXXN50	TO262
	AOTFXXN50	TO-220F
	AOTXXN50	TO-220
	AOBXXN50	TO263
	AODXXN50	TO252
	AOUXXN50	TO251

Note: Letter 'XX' is 1 or 2 digital which stands for Id (Continuous Drain current at 25°C) of this product.
For example, AOTF14N50, '14' means Id of this product is 14A.

Table 3 Reliability Test and Package test Result:

Test Item	Test Condition	Time Point	Total Sample size	Number of failure
HTGB	Temp = 150°c , Vgs=100% of Vgsmax	168 / 500 hrs 1000 hrs	2541	0
HTRB	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 hrs 1000 hrs	2464	0
Solder reflow precondition	168hr 85°c /85%RH + 3 cycle reflow @250°c /260°c (MSL level 1, peak temperature depending on package thickness and volume)	-	3839	0
HAST	130 +/- 2°C , 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	605	0
Pressure Pot	121°C , 29.7psi, 100%RH	96 hrs	1540	0
Temperature Cycle	-65°C to 150°C, air to air,	250 / 500 cycles	2002	0
Power Cycle	ΔTj=125°C	4286 cycles	231	0
Solder dunk	260°C, 10secs	3 cycles	77	0

Reliability Evaluation:

FIT rate (per billion): 1.74
MTTF = 65789 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate (FIT) = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**]** = 1.83 x 10^9 / **[**2 (2541) (168) (258) +2(1694) (500) (258) + 2(770) (1000) (258)**]** = 1.74

MTTF = 10^9 / FIT = 5.76 x 10^8hrs = 65789 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from HTRB and HTGB tests
H = Duration of HTRB/HTGB testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s]

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	**258**	**87**	**32**	**13**	**5.64**	**2.59**	**1**

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K