

AOS Semiconductor Product Reliability Report

AOZ1360AIL_4 & AOZ1364AIL rev B

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

475 Oakmead Parkway Sunnyvale, CA 94085 United States

> Tel: (408)830-9742 www.aosmd.com



The AOS product reliability report summarizes the qualification results for AOZ1360AIL_4/AOZ1364AIL in SO8 package. Accelerated environmental tests are performed on a specific sample size, samples are electrically tested before and after each stress time point. Review of final electrical test results confirm that AOZ1360AIL_4/AOZ1364AIL pass the AOS quality and reliability requirements. The released products will be categorized by its process family and routinely monitored for continuous improvement of product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Sample Size / Lots	Number of Failures	Reference Standard
HTOL	T _J = 150°C, V _{IN} = 28V	168 / 500 / 1000 hours	231 pcs (3 lots)	0	JESD22-A108
Preconditioning (Note A)	T _A = 85°C, RH = 85% + 3 cycle reflow @ 260°C (MSL 1)	168 hours	924 pcs (3 lots)	0	JESD22-A113
HAST	T _A = 130°C, RH = 85%, P = 33.3psia, V _{IN} = 28V	96 hours	231 pcs (3 lots)	0	JESD22-A110
Pre-con + PCT (autoclave)	121°C , 29.7psia, RH=100%	168 hours	231 pcs (3 lots)	0	JESD22-A102
Temperature Cycle	T₄ = -65°C to 150°C, air to air	250 / 500 / 1000 cycles	231 pcs (3 lots)	0	JESD22-A104
HTSL	T _A = 150°C	500 / 1000 hours	231 pcs (3 lots)	0	JESD22-A103

Note: The reliability data presents total of available generic data up to the published date. Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the product technology. Failure Rate Determination is based on JEDEC Standard JESD 85.

FIT rate (failures per billion device hours): 0.460 MTTF = 2,174.7 million hrs

The failure rate (λ) is calculated as follows:

$λ = χ^2$ [CL,(2f+2)] /2 x [1/(SS x t x AF)]; [equation 1]	where	CL = % of confidence level f = number of failure SS = sample size t = stress time
		t = stress time

Looking up the $\gamma^2/2$ table for zero failure (burn-in) with 60% confidence, the value of γ^2 [CL,(2f+2)]/2 is 0.92.

The Acceleration Factor (AF) is calculated from the following formula (both temperature and voltage acceleration factors are used in the final acceleration factor calculation) : $E_a = activation energy$

 $AF = AF_T x AF_V = exp[(E_a/k) x (1/T_0-1/T_s)] x exp[\beta (Vs-Vo)] where$

- k = Boltzmann constant
- $T_0 = operating T_J$
- $T_s = stress T_J$
- Vs = stress voltage
- V_o = operating voltage



 β = voltage acceleration coefficient

Assuming typical operating environment, $V_o = 25V$, $T_o = 55^{\circ}C$, $E_a = 0.7eV$, $V_{s(DriverIC)} = 28V$, $V_{s(MOSFET)} = 30V$, $T_s = 150^{\circ}C$, $\beta = 0.5$ (silicon defect)

$$AF(DriverIC) = \exp\left[\left(\frac{0.7}{8.617E - 5}\right) \bullet \left(\frac{1}{273 + 55} - \frac{1}{273 + 150}\right)\right] \bullet \exp[0.5 \bullet (28V - 25V)]$$
$$AF(MOSFET) = \exp\left[\left(\frac{0.7}{8.617E - 5}\right) \bullet \left(\frac{1}{273 + 55} - \frac{1}{273 + 150}\right)\right] \bullet \exp[0.5 \bullet (30V - 25V)]$$

Substituting the values in equation 1, we have $\lambda = 2 \cdot \lambda(MOSFET) + \lambda(DriverIC) =$

$$0.92 \bullet \frac{2}{\text{Sample Size} \bullet \text{Stress Duration} \bullet AF(\text{MOSFET})} + \frac{1}{\text{sample Size} \bullet \text{Stress Duration} \bullet AF(\text{DriverIC})} hr^{-1}$$

 λ = 0.460 10⁻⁹ hr ⁻¹ or 0.460 FIT; MTTF = (1/ λ) = 2,174.7 million hrs = 248,251 years

The calculation shows failure rate is 0.460 FIT, MTTF is 2,174.7 million hours under typical operating conditions.



TEST REPORT

Part Number: AOZ1360AIL_4 / AOZ1364AIL Package: SO8

ESD, LATCH UP RESULTS								
Test	Specification	Conditions	Temperature	Sample Size	Results			
Electrostatic Discharge	JESD-A114	±2.5kV (HBM)	25C	3	PASS			
Electrostatic Discharge	JESD-C101	±1kV (CDM)	25C	3	PASS			
Latch Up	JESD78	±100mA, 1.5x OV	25C	6	PASS			
Latch Up	JESD78	±100mA, 1.5x OV	125C	6	PASS			

Note:

1. ATE results are used to determine PASS/FAIL. Parametric shift <10%.

Pin Configuration:

