ALPHA & OMEGA SEMICONDUCTOR

Alpha & Omega Semiconductor Product Reliability Report

AOZ13987DI-02, rev D

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

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This AOS product reliability report summarizes the qualification result for AOZ13987DI-02. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOZ13987DI-02 using TP004E8 version meet requirements as extension qualification. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTOL (TP004E6 and TP004E8)	Temp = 125°C, Vcc=Vccmax	168 / 500 / 1000 hours and 168hours	240 pcs 80 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	960 pcs	0	JESD22-A113
HAST (Note 1)	130°C, RH = 85%, 33.3 psia, Vcc= Vccmax	96 hours	240 pcs	0	JESD22-A110
Autoclave	121°C , 29.7psia, RH=100%	96 hours	240pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C, air to air	250 / 500 cycles	240 pcs	0	JESD22-A104
High Temperature storage (Note1)	150°C	168 hours	240pcs	0	JESD22-A103

Note A:
MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation
FIT rate (per billion): 13.91
MTTF = 8206 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**] =** 13.91
MTTF = 10^9 / FIT = 8206 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]

Acceleration Factor ratio list:

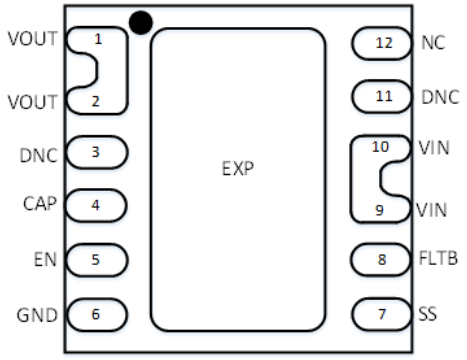
	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	125 deg C
Af	77	26	9.8	3.9	1.7	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K

III. ESD and Latch Up Test Results

Test	Test Conditions	Total Sample Size	Number of Failures	Reference Standard
Electrostatic Discharge Human Body Model	**T_A = 25°C, +/-4kV**	**3**	**0**	**JESD-A114**
Electrostatic Discharge Charged Device Model	**T_A = 25°C, +/-1kV**	**3**	**0**	**JESD-C101**
Electrostatic Discharge Immunity (only VIN pin)	**T_A = 25°C, +/-8kV**	**3**	**0**	**IEC61000-4-2**
Electrostatic Discharge Surge test (only VIN pin)	**T_A = 25°C, 40V**	**3**	**0**	**IEC61000-4-5**
Latch Up	**T_A = 25°C, +/-100mA, 1.5x OV**	**6**	**0**	**JESD78**
Latch Up	**T_A = 125°C, +/-100mA, 1.5x OV**	**6**	**0**	**JESD78**

(1) ATE results are used to determine PASS/FAIL. Parametric shift <10%.



3mm x 3mm DFN-12L
(Top Transparent View)