AOS Semiconductor
Product Reliability Report

AOZ6682CI/AOZ6683CI, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

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ALPHA & OMEGA SEMICONDUCTOR

This AOS product reliability report summarizes the qualification result for AOZ6682/83CI. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOZ6682/83CI passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTOL	T_J = 125°C, V_{IN} = V_{IN} max	168 / 500 / 1000 hours	231 pcs	0	JESD22-A108
Preconditioning (Note A)	T_A = 85°C, RH = 85% + 3 cycle reflow @ 260°C (MSL 1)	-	924 pcs	0	JESD22-A113
HAST	T_A = 130°C, RH = 85%, P = 33.3psia, V_{IN} = V_{IN} max	96 hours	231 pcs	0	JESD22-A110
Autoclave	T_A = 121°C, RH = 100%, P = 29.7psia	168 hours	231 pcs	0	JESD22-A102
Temperature Cycle	T_A = -65°C to 150°C, air to air	1000cycles	231 pcs	0	JESD22-A104
HTSL	T_A = 150°C	1000 hours	231 pcs	0	JESD22-A103

Note: The reliability data presents total of available generic data up to the published date.
Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

Taking the result of HTOL AOZ6682CI & AOZ6683CI Lots the total device stress time

FIT rate (per billion): 15.26 FIT
MTTF = 7480 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/** **[**2 (N) (H) (Af)**] =** 15.26
MTTF = 10^9 / FIT = 7480 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and T_{use} = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** ($1/T_J u - 1/T_J s$)]
Acceleration Factor ratio list:

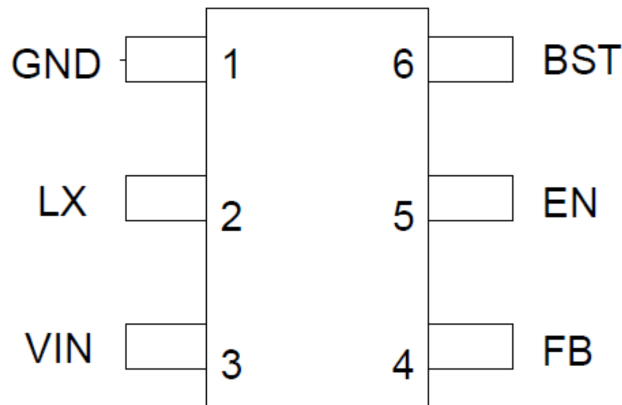
	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	125 deg C
Af	77	26	9.8	3.9	1.7	1

T_J s = Stressed junction temperature in degree (Kelvin), K = C + 273.16
T_J u =The use junction temperature in degree (Kelvin), K = C + 273.16
k = Boltzmann's constant, 8.617164×10^{-5}eV / K

III. ESD and Latch Up Test Results

Test	Test Conditions	Total Sample Size	Number of Failures	Reference Standard
Electrostatic Discharge Human Body Model	T_A = 25°C, +/-2kV	3	0	JESD-A114
Electrostatic Discharge Charged Device Model	T_A = 25°C, +/-1kV	3	0	JESD-C101
Latch Up	T_A = 25°C, +/-100mA, 1.5x OV	6	0	JESD78
Latch Up	T_A = 85°C, +/-100mA, 1.5x OV	6	0	JESD78

(1) ATE results are used to determine PASS/FAIL. Parametric shift<10%.



Top Transparent View

6-pin SOT23-6